REMARKS

The present application was filed on April 9, 2004 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Masiewicz (United States Patent Number 5,632,019).

The specification has been amended to correct typographical errors.

Independent Claims 1, 8 and 19

Independent claims 1, 8, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Masiewicz. In particular, the Examiner asserts that Masiewicz discloses "advantages to sensing a bus load variation, which includes detecting an added bus receiver on a computer system bus, by detecting the rate of voltage change on the bus in response to an injected current." The Examiner acknowledges that Masiewicz "does not discuss adjusting a common mode voltage by the current injection, and does not mention application of the load-sensing to a PCI-Express link," but asserts that "Official Notice is taken that PCI-Express was a well-known kind of computer system bus at the time the invention was made."

Applicants note that the Examiner did not cite any particular passages of Masiewicz in rejecting the claims. Applicants note, however, that Masiewicz teaches that,

> if desired, a load sense element 102 may be provided to sense the capacitive load C_L coupled to the output of the programmable buffer 20. In computer systems wherein SCSI-compatible hard disc units, e.g., units 6, are driven by a host computer (e.g., 4), a ***polling function*** *is available to indicate how many hard disc units are present*. Using this polling information, load sense 102 and microprocessor 100 can collectively program the driver control logic. For example, if polling indicates three hard disc units are present, information available to microprocessor 100, perhaps from an associated look-up table, could determine the desired programming mode to be implemented for output buffer 20. Such programming could include the number of unit buffers to be used, the type of cascading, if any, to be used, and so forth
>
> In applications wherein polling or the equivalent function does not normally exist, *load sense 102 could include circuitry to* ***approximate the effective C_L to be driven***. Load sense 102 could, for example, include a constant reference current source I_{REF} and a voltage sense circuit. Since the voltage v(t) developed across C_L due to I_{REF} will be:

$$V(t) = \frac{I_{REF}}{C_L} \int dt$$

C_L may be determined by the magnitude of v(t) developed in a given amount of time. Of course, other methods for sensing C_L are also possible.
(Col. 12, lines 12-39; emphasis added.)

First, contrary to the Examiner's assertion, Applicants find ***no*** disclosure or suggestion of "*detecting an added bus receiver* on a computer system bus, *by detecting the rate of voltage change on the bus* in response to an injected current." Second, as the Examiner acknowledges, Masiewicz does ***not*** disclose or suggest adjusting a common mode voltage by the current injection, and does ***not*** mention application of the load-sensing to a PCI-Express link. Finally, Masiewicz does ***not*** disclose or suggest *adjusting a common mode voltage by injecting a current* into one or more transmitter output nodes; and does ***not*** disclose or suggest *detecting whether a receiver is present* on said PCI-Express link based on a voltage change rate. Independent claims 1, 8, and 19 require adjusting a common mode voltage by injecting a current into one or more transmitter output nodes; and detecting whether a receiver is present on said PCI-Express link based on a voltage change rate.

Thus, Masiewicz does not disclose or suggest adjusting a common mode voltage by injecting a current into one or more transmitter output nodes; and detecting whether a receiver is present on said PCI-Express link based on a voltage change rate, as required by independent claims 1, 8, and 19.

Dependent Claims 2-7, 9-18 and 20

Dependent claims 2-7, 9-18 and 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Masiewicz.

Claims 2-7, 9-18 and 20 are dependent on claims 1, 8, and 19, respectively, and are therefore patentably distinguished over Masiewicz because of their dependency from independent claims 1, 8, and 19 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i e , claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

Date: January 24, 2007

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